

# SN54ABT16843, SN74ABT16843 18-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), 300-mil Shrink Small-Outline (DL) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

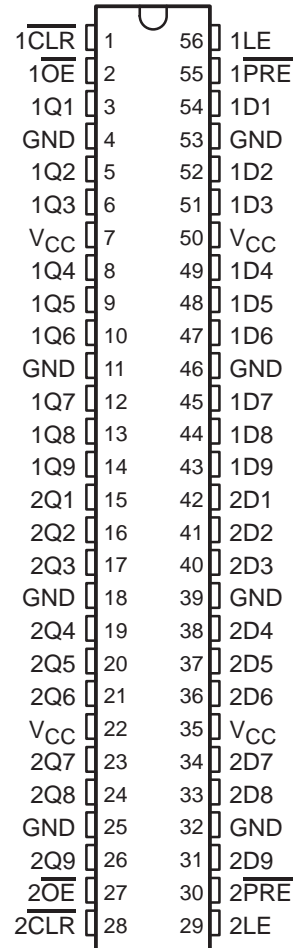
## description

The 'ABT16843 18-bit bus-interface D-type latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ABT16843 can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device provides true data at its outputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs are in the high-impedance state during power up and power down. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54ABT16843 . . . WD PACKAGE  
SN74ABT16843 . . . DGG OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus and EPIC-II B are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

**SN54ABT16843, SN74ABT16843**  
**18-BIT BUS-INTERFACE D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

**description (continued)**

$\overline{OE}$  does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16843 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT16843 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**  
 (each 9-bit latch)

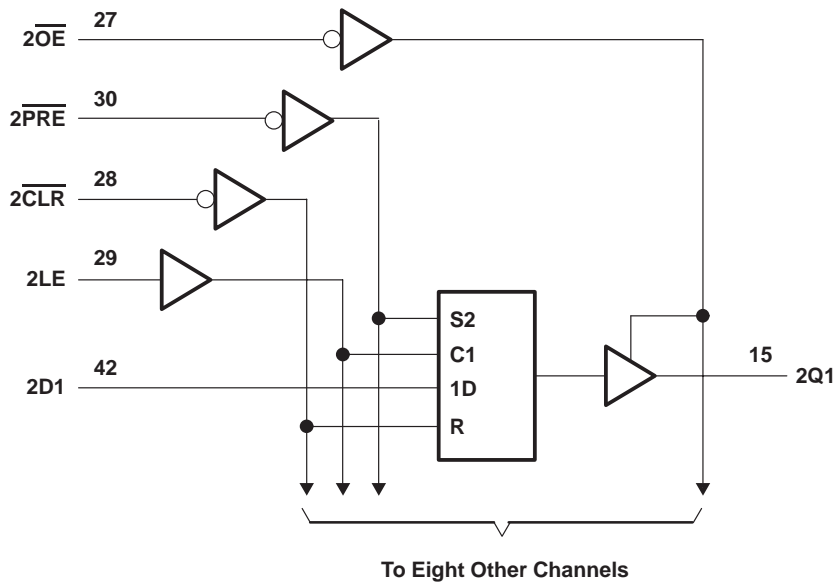
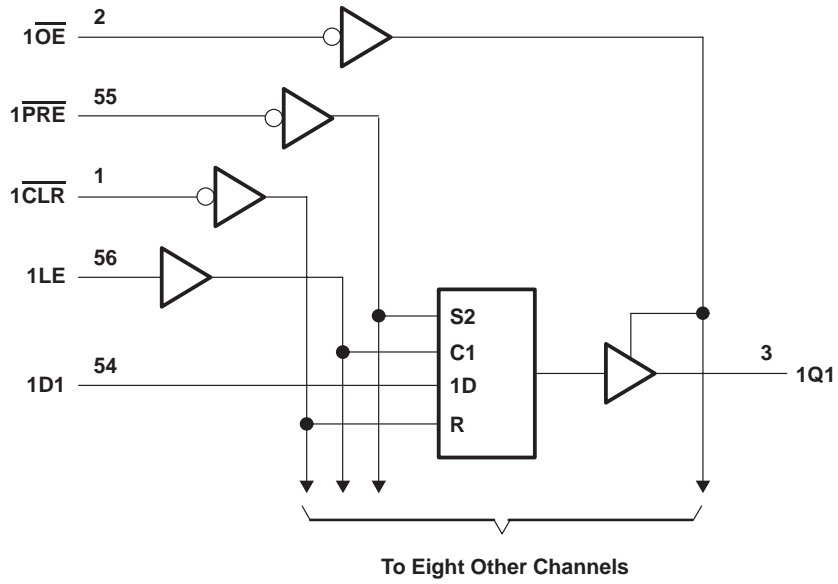
| INPUTS           |                  |                 |    |   | OUTPUT<br>Q |
|------------------|------------------|-----------------|----|---|-------------|
| $\overline{PRE}$ | $\overline{CLR}$ | $\overline{OE}$ | LE | D |             |
| L                | X                | L               | X  | X | H           |
| H                | L                | L               | X  | X | L           |
| H                | H                | L               | H  | L | L           |
| H                | H                | L               | H  | H | H           |
| H                | H                | L               | L  | X | $Q_0$       |
| X                | X                | H               | X  | X | Z           |



SN54ABT16843, SN74ABT16843  
 18-BIT BUS-INTERFACE D-TYPE LATCHES  
 WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

logic diagram (positive logic)



# SN54ABT16843, SN74ABT16843

## 18-BIT BUS-INTERFACE D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$  | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT16843            | 96 mA           |
| SN74ABT16843  | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package        | 81°C/W          |
| DL package  | 74°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

#### recommended operating conditions (see Note 3)

|  | SN54ABT16843    |          | SN74ABT16843 |          | UNIT |
|--|-----------------|----------|--------------|----------|------|
|  | MIN             | MAX      | MIN          | MAX      |      |
| $V_{CC}$ Supply voltage                                | 4.5             | 5.5      | 4.5          | 5.5      | V    |
| $V_{IH}$ High-level input voltage                      | 2               |          | 2            |          | V    |
| $V_{IL}$ Low-level input voltage                       |                 | 0.8      |              | 0.8      | V    |
| $V_I$ Input voltage                                    | 0               | $V_{CC}$ | 0            | $V_{CC}$ | V    |
| $I_{OH}$ High-level output current                     |                 | –24      |              | –32      | mA   |
| $I_{OL}$ Low-level output current                      |                 | 48       |              | 64       | mA   |
| $\Delta t/\Delta v$ Input transition rise or fall rate | Outputs enabled |          | 10           | 10       | ns/V |
| $\Delta t/\Delta V_{CC}$ Power-up ramp rate            | 200             |          | 200          |          | μs/V |
| $T_A$ Operating free-air temperature                   | –55             | 125      | –40          | 85       | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# SN54ABT16843, SN74ABT16843 18-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                | TEST CONDITIONS  | T <sub>A</sub> = 25°C   |      |       | SN54ABT16843 |      | SN74ABT16843 |      | UNIT |
|--------------------------|--|---|------|-------|--------------|------|--------------|------|------|
|                          |  | MIN   | TYP† | MAX   | MIN          | MAX  | MIN          | MAX  |      |
| V <sub>IK</sub>          | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                       |   |      | -1.2  |              | -1.2 |              | -1.2 | V    |
| V <sub>OH</sub>          | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                       |   | 2.5  |       | 2.5          |      | 2.5          |      | V    |
|                          | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA   |   | 3    |       | 3            |      | 3            |      |      |
|                          | V <sub>CC</sub> = 4.5 V  | I <sub>OH</sub> = -24 mA  |      | 2     |              | 2    |              |      |      |
| I <sub>OH</sub> = -32 mA |  |   | 2*   |       |              |      | 2            |      |      |
| V <sub>OL</sub>          | V <sub>CC</sub> = 4.5 V  | I <sub>OL</sub> = 48 mA   |      | 0.55  |              | 0.55 |              |      | V    |
|                          |  | I <sub>OL</sub> = 64 mA   |      | 0.55* |              |      | 0.55         |      |      |
| V <sub>hys</sub>         |  |   | 100  |       |              |      |              |      | mV   |
| I <sub>I</sub>           | V <sub>CC</sub> = 0 to 5.5 V,<br>V <sub>I</sub> = V <sub>CC</sub> or GND               |   |      | ±1    |              | ±1   |              | ±1   | μA   |
| I <sub>OZPU</sub> ‡      | V <sub>CC</sub> = 0 to 2.1 V,<br>V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$  |   |      | ±50   |              | ±50  |              | ±50  | μA   |
| I <sub>OZPD</sub> ‡      | V <sub>CC</sub> = 2.1 V to 0,<br>V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$  |   |      | ±50   |              | ±50  |              | ±50  | μA   |
| I <sub>OZH</sub>         | V <sub>CC</sub> = 2.1 V to 5.5 V,<br>V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V  |   |      | 10    |              | 10   |              | 10   | μA   |
| I <sub>OZL</sub>         | V <sub>CC</sub> = 2.1 V to 5.5 V,<br>V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V  |   |      | -10   |              | -10  |              | -10  | μA   |
| I <sub>off</sub>         | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                          |   |      | ±100  |              |      |              | ±100 | μA   |
| I <sub>CEX</sub>         | Outputs high<br>V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                        |   |      | 50    |              | 50   |              | 50   | μA   |
| I <sub>O</sub> §         | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V  | -50   | -100 | -180  | -50          | -180 | -50          | -180 | mA   |
| I <sub>CC</sub>          | Outputs high   |   |      | 0.5   |              | 0.5  |              | 0.5  | mA   |
|                          | Outputs low  | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0,<br>V <sub>I</sub> = V <sub>CC</sub> or GND |      | 85    |              | 85   |              | 85   |      |
|                          | Outputs disabled   |   |      | 0.5   |              | 0.5  |              | 0.5  |      |
| ΔI <sub>CC</sub> ¶       | V <sub>CC</sub> = 5.5 V, One input at 3.4 V,<br>Other inputs at V <sub>CC</sub> or GND |   |      | 1.5   |              | 1.5  |              | 1.5  | mA   |
| C <sub>i</sub>           | V <sub>I</sub> = 2.5 V or 0.5 V  |   |      | 3.5   |              |      |              |      | pF   |
| C <sub>o</sub>           | V <sub>O</sub> = 2.5 V or 0.5 V  |   |      | 8     |              |      |              |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ABT16843, SN74ABT16843**  
**18-BIT BUS-INTERFACE D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

SCBS223E – OCTOBER 1992 – REVISED MAY 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|                 |                             | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     | SN54ABT16843 |     | SN74ABT16843 |     | UNIT |
|-----------------|-----------------------------|---|-----|--------------|-----|--------------|-----|------|
|                 |                             | MIN   | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>w</sub>  | Pulse duration              | CLR low   | 3.3 | 3.3          | 3.3 | 3.3          | ns  |      |
|                 |                             | PRE low   | 3.3 | 3.3          | 3.3 |              |     |      |
|                 |                             | LE high   | 3.3 | 3.3          | 3.3 |              |     |      |
| t <sub>su</sub> | Setup time, data before LE↓ | High  | 0.9 | 0.9          | 0.9 | ns           |     |      |
|                 |                             | Low   | 0.6 | 0.6          | 0.6 |              |     |      |
| t <sub>h</sub>  | Hold time, data after LE↓   | High  | 1.7 | 1.7          | 1.7 | ns           |     |      |
|                 |                             | Low   | 1.8 | 1.8          | 1.8 |              |     |      |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

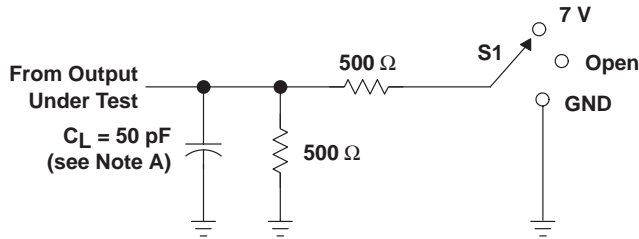
| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | SN54ABT16843 |     | SN74ABT16843 |     | UNIT |
|------------------|-----------------|----------------|---|-----|-----|--------------|-----|--------------|-----|------|
|                  |                 |                | MIN   | TYP | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>PLH</sub> | D               | Q              | 1.6   | 3.1 | 4.2 | 1.6          | 5.1 | 1.6          | 4.8 | ns   |
| t <sub>PHL</sub> |                 |                | 1.6   | 3.2 | 4.2 | 1.6          | 5   | 1.6          | 4.8 |      |
| t <sub>PLH</sub> | LE              | Q              | 2.3   | 4   | 5   | 2.3          | 6.3 | 2.3          | 5.9 | ns   |
| t <sub>PHL</sub> |                 |                | 2.5   | 3.9 | 4.8 | 2.5          | 5.6 | 2.5          | 5.3 |      |
| t <sub>PLH</sub> | PRE             | Q              | 2.1   | 4   | 5.1 | 2.1          | 6.3 | 2.1          | 6.1 | ns   |
| t <sub>PHL</sub> |                 |                | 2.2   | 3.7 | 4.6 | 2.2          | 5.3 | 2.2          | 5   |      |
| t <sub>PLH</sub> | CLR             | Q              | 1.9   | 3.7 | 4.8 | 1.9          | 5.7 | 1.9          | 5.4 | ns   |
| t <sub>PHL</sub> |                 |                | 2.2   | 4.2 | 5.3 | 2.2          | 6.1 | 2.2          | 6   |      |
| t <sub>PZH</sub> | OE              | Q              | 1.6   | 3.3 | 4.3 | 1.6          | 5.5 | 1.6          | 5.4 | ns   |
| t <sub>PZL</sub> |                 |                | 2   | 3.2 | 4.6 | 2            | 5.9 | 2            | 5.8 |      |
| t <sub>PHZ</sub> | OE              | Q              | 1.7   | 4   | 5.5 | 1.7          | 6.4 | 1.7          | 6.3 | ns   |
| t <sub>PLZ</sub> |                 |                | 1.7   | 3.7 | 4.4 | 1.7          | 5.3 | 1.7          | 5.2 |      |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



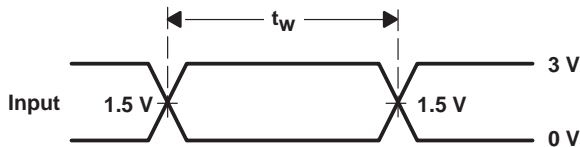
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

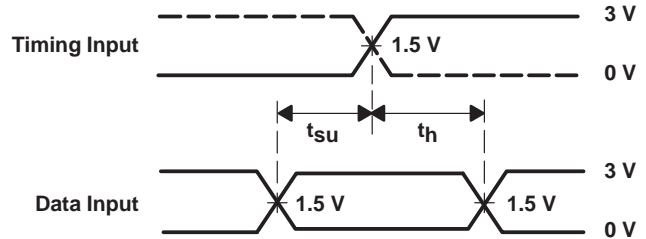


LOAD CIRCUIT

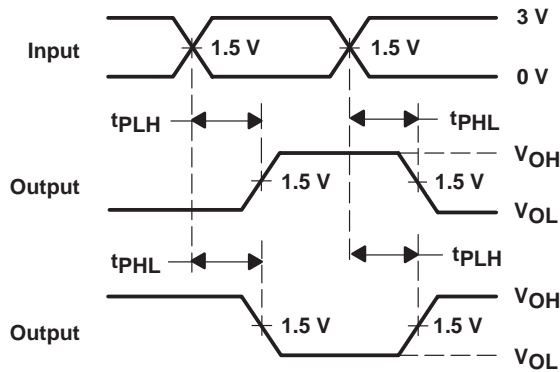
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



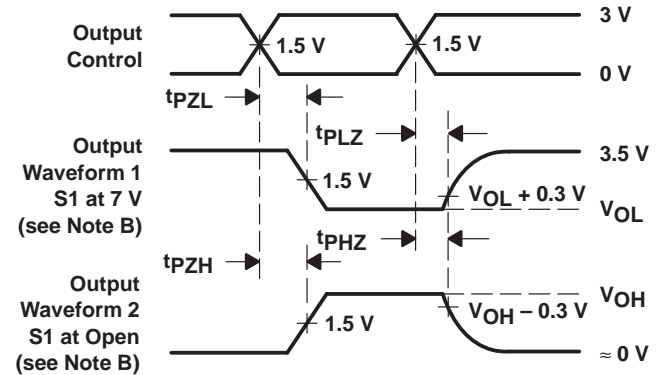
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16843DGGR | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74ABT16843DLR  | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT16843DGGR | TSSOP        | DGG             | 56   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74ABT16843DLR  | SSOP         | DL              | 56   | 1000 | 346.0       | 346.0      | 49.0        |

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

|                             |  |
|-----------------------------|--|
| Amplifiers                  | <a href="http://amplifier.ti.com">amplifier.ti.com</a>             |
| Data Converters             | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     |
| DSP                         | <a href="http://dsp.ti.com">dsp.ti.com</a>                         |
| Clocks and Timers           | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>           |
| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             |
| Logic                       | <a href="http://logic.ti.com">logic.ti.com</a>                     |
| Power Mgmt                  | <a href="http://power.ti.com">power.ti.com</a>                     |
| Microcontrollers            | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> |
| RFID                        | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>               |
| RF/IF and ZigBee® Solutions | <a href="http://www.ti.com/lprf">www.ti.com/lprf</a>               |

### Applications

|                    |  |
|--------------------|--|
| Audio              | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                   |
| Automotive         | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| Broadband          | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Digital Control    | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Medical            | <a href="http://www.ti.com/medical">www.ti.com/medical</a>               |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Optical Networking | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
| Telephony          | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
| Video & Imaging    | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
| Wireless           | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated